ACME: An Architecture Compiler for Model Emulation

Colin J. Ihrig, Rami Melhem, and Alex K. Jones
University of Pittsburgh
cji3@pitt.edu, melhem@cs.pitt.edu, akjones@ece.pitt.edu

Abstract

Simulation of new many-core systems is becoming an increasingly large bottleneck in the design process. This work presents the ACME design automation tool flow that facilitates the hardware emulation of newly proposed large multi-core interconnection networks on FPGAs to mitigate the slowdowns of single threaded event driven simulation. The tool is aimed at computer and network architects who have knowledge of digital design but may not be comfortable with hardware description languages and synthesis flows. ACME uses a graphical entry that allows a mix of hardware components with software algorithms written in C, each with a user defined latency and throughput in terms of target system clock cycles. The designs can be simulated for correctness in software and then ACME automatically generates a cycle accurate hardware emulator as a Xilinx Platform Studio project, which integrates synthesized hardware blocks with embedded soft-core processors that execute the C code. The results demonstrate that for a 16-core and 64-core cycle accurate packet switching network the FPGA-based emulation is faster than Simics-based software simulation by 4x and 23.5x, respectively.

I. SUBMISSION INFORMATION

YouTube link:
http://www.youtube.com/watch?v=DcAOiqGgYBA

Supporting publication:
Automated Modeling and Emulation of Interconnect Designs for Many-Core Chip Multiprocessors, appearing in the DAC 2010 proceedings.

For additional correspondence, please contact Colin Ihrig at cji3@pitt.edu.